Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 42461

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018

Sixth Semester

Electronics and Communication Engineering

EC2354 – VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008)

(Also Common to PTEC2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – ECE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Define threshold voltage of a MOS transistor.
2. State the purpose of design rules.
3. Define logical effort.
4. What is meant by design or process corners ?
5. State the logics by which low power circuit designs can be realised.
6. What is a keeper circuit ?
7. What is the need for testing in integrated circuits ?
8. State the general types of fixtures used to test a chip.
9. What is a Net in Verilog ? What is its default value ?
10. Write the verilog code to realise a 2 to 1 MUX using gate level modelling.

PART – B **(5×16=80 Marks)**

11. a) Derive and explain the expression for drain current of a nMOS transistor.

(OR)

b) Discuss the various steps involved in the fabrication of a CMOS transistor.

12. a) Explain the different types of power dissipation in a CMOS circuit and explain briefly the methods to reduce these powers.

(OR)

b) Discuss, in detail, the reliability problems that cause integrated circuits to fail permanently.

13. a) Explain the working of cascade voltage switch logic with an example. State its advantages and disadvantages.

(OR)

b) Explain the methods of sequencing blocks of combinational logic. Explain also on maximum and minimum delay constraints that have to be adhered to in one of the above methods.

14. a) Explain on the logics of the following methods of testing logic circuits :

i) Automatic test pattern generation

ii) Adhoc testing

iii) Built-in self test

iv) IDDQ testing. **(4×4=16)**

(OR)

b) i) Define observability and controllability. **(4)**

ii) Explain, in detail on boundary scan testing. **(12)**

15. a) i) Explain the components of a verilog module. **(8)**

ii) Explain tasks and functions in verilog. **(8)**

(OR)

b) i) What are block statements ? How many types of blocks are supported by verilog for a ripple carry counter ? **(6)**

ii) Convert a D flip flop into T flip flop. Design a 4 bit ripple carry counter using T flip-flops and write the verilog code using hierarchical model. **(10)**
